1. A diode, said diode comprising:

an isolation region formed in a substrate;

a first doped active layer of a first conductivity type formed in said substrate, wherein said doped layer is spaced apart from said isolation region; and

a second doped active layer of a second conductivity type in contact with said first doped active layer, the contact of said first and second active layers forming a p-n junction.

2. The diode according to claim 1, wherein the first conductivity type is n-type, and the second conductivity type is p-type.

3. The diode according to claim 1, wherein said isolation region is a field oxide region formed by the Local Oxidation of Silicon process.

4. The diode according to claim 1, wherein said isolation region is a field oxide region formed by the Shallow Trench Isolation process.

5. The diode according to claim 1, wherein said first doped active layer is spaced from said isolation region by from about 0.05 μm to about 1.0 μm.

6. The diode according to claim 5, wherein said first doped active layer is spaced from said isolation region by about 0.1 μm to about 0.8 μm.

7. The diode according to claim 6, wherein said first doped active layer is spaced from said isolation region by about 0.2 to 0.7 μm.

8. The diode according to claim 1, further comprising a first doped region of a second conductivity type at least partially under said isolation region.

9. The diode according to claim 8, wherein said first doped region is spaced away from the edge of said isolation region.

10. The diode according to claim 8, wherein said first doped region is a p-type region.

11. The diode according to claim 1, wherein said first doped active layer is doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

12. The diode according to claim 11, wherein said first doped active layer is doped with phosphorous.

13. The diode according to claim 11, wherein said first doped active layer is doped at a dopant dose of from about $1x10^{11}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2.

14. The diode according to claim 8, wherein said first doped region is doped at a dopant dose of from about $1x10^{11}$ ions/cm^2 to about $1x10^{14}$ ions/cm^2.

15. The diode according to claim 1, wherein said first doped active layer is an n-type active layer and said second doped active layer is a p-well.

16. The diode according to claim 1, further comprising a third doped active layer at least partially within said first doped active layer.

17. The diode according to claim 16, wherein said third doped active layer is spaced away from the edge of said first doped active layer.

18. The diode according to claim 16, wherein said third doped active layer is an n-type region.

19. The diode according to claim 16, wherein said third doped active layer is doped at a dopant dose of from about $1x10^{12}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2.

20. The diode according to claim 9, further comprising a third doped active layer at least partially within said first doped active layer.

21. The diode according to claim 20, wherein said third doped active layer is spaced away from the edge of said first doped active layer.

22. The diode according to claim 20, wherein said third doped active layer is an n-type region.

23. The diode according to claim 20, wherein said third doped active layer is doped at a dopant dose of from about $1x10^{12}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2.

24. The diode according to claim 1, wherein said diode is used in a CCD imager array.

25. The diode according to claim 1, wherein said diode is used in a CMOS imager array.

26. The diode according to claim 1, wherein said diode is used in a memory array.

27. The diode according to claim 1, wherein said diode is used in a logic device.

28. A diode for use in an imaging device, said diode comprising:

an isolation region formed in a substrate;

a first doped active layer of a first conductivity type formed in said substrate of a second conductivity type, wherein said first doped active layer is spaced apart from said isolation region; and

a second doped active layer of a first conductivity type formed within said first doped active layer, wherein said second doped active layer is doped to a higher dopant

dose that said first doped active layer, wherein said first and second active layers and said substrate form a p-n junction.

29. The diode according to claim 28, wherein the first conductivity type is n-type, and the second conductivity type is p-type.

30. The diode according to claim 28, wherein said isolation region is a field oxide region formed by the Local Oxidation of Silicon.

31. The diode according to claim 28, wherein said isolation region is a field oxide region formed by the Shallow Trench Isolation process.

32. The diode according to claim 28, wherein said first doped active layer is spaced from said isolation region by from about 0.05 μm to about 1.0 μm.

33. The diode according to claim 28, wherein said first doped active layer is spaced from said isolation region by about 0.1 μm to about 0.8 μm.

34. The diode according to claim 28, wherein said first doped active layer is spaced from said isolation region by about 0.2 μm to about 0.7 μm.

35. The diode according to claim 28, further comprising a first doped region of a second conductivity type under said isolation region.

36. The diode according to claim 35, wherein said first doped region is spaced away from the edge of said isolation region.

37. The diode according to claim 35, wherein said first doped region is a p-type region

38. The diode according to claim 28, wherein said first doped active layer is doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

39. The diode according to claim 38, wherein said first doped active layer is doped with phosphorous.

40. The diode according to claim 28, wherein said second doped active layer is doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

41. The diode according to claim 40, wherein said second doped active layer is doped with phosphorous.

42. The diode according to claim 28, wherein said first doped active layer is doped at a dopant dose of from about $1x10^{11}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2.

43. The diode according to claim 28, wherein said second doped active layer is doped at a dopant dose of from about $1x10^{11}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2.

44. The diode according to claim 35, wherein said first doped region is doped at a dopant dose of from about $1x10^{11}$ ions/cm^2 to about $1x10^{14}$ ions/cm^2.

45. The diode according to claim 28, wherein said first doped active layer is an n- region and said second doper active layer is an n+ region.

46. The diode according to claim 28, wherein said diode is used in a CCD imager array.

47. The diode according to claim 28, wherein said diode is used in a CMOS imager array.

48. The diode according to claim 28, wherein said diode is used in a memory array.

49. The diode according to claim 28, wherein said diode is used in a logic device.

50. An imager device comprising:

(i) a processor; and

(ii) an imaging device coupled to said processor, said imaging device comprising:

a photodiode for use in an imaging device, said photodiode comprising:

an isolation region formed in a substrate;

a first doped photoactive layer of a first conductivity type formed in said substrate, wherein said doped layer is spaced apart from said isolation region; and

a second doped photoactive layer of a second conductivity type in contact with said first doped photoactive layer, the contact of said first and second photoactive layers forming a p-n junction.

51. The imager according to claim 50, wherein the first conductivity type is n-type, and the second conductivity type is p-type.

52. The imager according to claim 50, wherein said isolation region is a field oxide region.

53. The imager according to claim 50, wherein said isolation region is a Shallow Trench Isolation region.

54. The imager according to claim 50, wherein said isolation region is formed of Local Oxidation of Silicon.

55. The imager according to claim 50, wherein said first doped photoactive layer is spaced from said isolation region by from about 0.05 μm to about 1.2 μm.

56. The imager according to claim 55, wherein said first doped photoactive layer is spaced from said isolation region by about 0.1 μm to about 0.8 μm.

57. The imager according to claim 50, wherein said first doped photoactive layer is spaced from said isolation region by about 0.2 μm to about 0.7 μm.

58. The imager according to claim 50, further comprising a first doped region of a second conductivity type under said isolation region.

59. The diode according to claim 57, wherein said first doped region is spaced away from the edge of said isolation region.

60. The imager according to claim 58, wherein said first doped region is a p-type region.

61. The imager according to claim 50, wherein said first doped photoactive layer is doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

62. The imager according to claim 67, wherein said first doped photoactive layer is doped with phosphorous.

63. The imager according to claim 67, wherein said first doped photoactive layer is doped at a dopant dose of from about $1x10^{11}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2.

64. The imager according to claim 58, wherein said first doped region is doped at a dopant dose of from about $1x10^{11}$ ions/cm^2 to about $1x10^{14}$ ions/cm^2.

65. The imager according to claim 50, wherein said imager is a CCD imager.

66. The imager according to claim 50, wherein said imager is a CMOS imager array.

67. An imager device comprising:

(i) a processor; and

(ii) an imaging device coupled to said processor, said imaging device comprising:

a photodiode for use in an imaging device, said photodiode comprising:

an isolation region formed in a substrate;

a first doped photoactive layer of a first conductivity type formed in said substrate doped to a second conductivity type, wherein said first doped photoactive layer is spaced apart from said isolation region; and

a second doped photoactive layer of a first conductivity type formed within said first doped photoactive layer, wherein said second doped photoactive layer is doped to a higher dopant dose that said first doped photoactive layer,

wherein said first and second photoactive layers and said substrate form a p-n junction.

68. The imager according to claim 67, wherein the first conductivity type is n-type, and the second conductivity type is p-type.

69. The imager according to claim 67, wherein said isolation region is a field oxide region.

70. The imager according to claim 67 herein said isolation region is a Shallow Trench Isolation region.

71. The imager according to claim 67 herein said isolation region is formed of Local Oxidation of Silicon.

72. The imager according to claim 67 wherein said first doped photoactive layer is spaced from said isolation region by from about 0.05 μm to about 1.2 μm.

73. The imager according to claim 67 herein said first doped photoactive layer is spaced from said isolation region by about 0.1 μm to about 0.8 μm.

74. The imager according to claim 67 wherein said first doped photoactive layer is spaced from said isolation region by about 0.2 μm to about 0.7 μm.

75. The imager according to claim 67, further comprising a first doped region of a second conductivity type under said isolation region.

76. The imager according to claim 75, wherein said first doped region is spaced away from the edge of said isolation region.

77. The imager according to claim 75, wherein said first doped region is a p-type region.

78. The imager according to claim 67, wherein said first doped photoactive layer is doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

79. The imager according to claim 78, wherein said first doped photoactive layer is doped with phosphorous.

80. The imager according to claim 67, wherein said second doped photoactive layer is doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

81. The imager according to claim 80, wherein said second doped photoactive layer is doped with phosphorous.

82. The imager according to claim 80, wherein said first doped photoactive layer is doped at a dopant dose of from about $1x10^{11}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2.

83. The imager according to claim 82, wherein said second doped photoactive layer is doped at a dopant dose of from about $1x10^{12}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2.

84. The imager according to claim 77, wherein said first doped region is doped at a dopant dose of from about $1x10^{11}$ ions/cm^2 to about $1x10^{14}$ ions/cm^2.

85. The imager according to claim 67, wherein said first doped photoactive layer is an n- region and said second doper photoactive layer is an n+ region.

86. The imager according to claim 67, wherein said imager is a CCD imager.

87. The imager according to claim 67, wherein said imager is a CMOS imager.

88. A method of forming a photodiode structure in a substrate, said method comprising the steps of:

forming an isolation region in said substrate;

forming a doped region of a first conductivity under said isolation region;

forming a doped photoactive layer of a second conductivity in said substrate, wherein said doped photoactive layer is spaced apart from said isolation region.

89. The method according to claim 88, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

90. The method according to claim 88, wherein the semiconductor substrate is a silicon substrate.

91. The method according to claim 88, wherein the doping step comprises ion implantation.

92. The method according to claim 91, wherein said doped photoactive layer is doped with a dopant selected from the group consisting of arsenic, antimony and phosphorous.

93. The method according to claim 92, wherein said doped photoactive layer is doped at a dopant dose level of from about $1x10^{11}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2.

94. The method according to claim 93, wherein said doped photoactive layer is spaced from said isolation regions by applying a mask to said substrate.

95. The method according to claim 93, wherein said doped photoactive layer and said doped regions are formed sequentially in said substrate with a single mask and resist.

96. A method of forming a photodiode in a substrate, said method comprising the steps of:

forming an isolation region in said substrate;

forming a doped region of a first conductivity under said isolation region;

forming a first doped photoactive layer of a second conductivity in said substrate encompassed by said isolation region, wherein said first doped photoactive layer is spaced apart from said isolation region; and

forming a second doped photoactive layer of a second conductivity within said first doped photoactive layer, wherein said second doped photoactive layer is doped at a dopant dose that is greater than said first doper photoactive layer.

97. The method according to claim 96, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

98. The method according to claim 96, wherein the semiconductor substrate is a silicon substrate.

99. The method according to claim 96, wherein the doping step comprises ion implantation.

100. The method according to claim 99, wherein said first doped photoactive layer is doped with a dopant selected from the group consisting of arsenic, antimony and phosphorous.

101. The method according to claim 100, wherein said first doped photoactive layer is doped at a dopant dose level of from about $1x10^{11}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2.

102. The method according to claim 101, wherein said second doped photoactive layer is doped with a dopant selected from the group consisting of arsenic, antimony and phosphorous.

103. The method according to claim 102, wherein said second doped photoactive layer is doped at a dopant dose level of from about $1x10^{11}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2.

104. The method according to claim 101, wherein said first doped photoactive layer is spaced from said isolation regions by applying a mask to said substrate.

105. The method according to claim 101, wherein said first doped photoactive layer and said doped regions are formed sequentially in said substrate with a single mask and resist.